REMARKS

Claims 1-11 have been examined, claims 6, 8, and 11 are cancelled, and claims 7 and 10 are amended. Accordingly, claims 1-5, 7, and 9-10 are now pending in the application. Reexamination and reconsideration of all outstanding rejections and objections are requested.

Claims 1, 3 and 5 are rejected under 35 U.S.C. §103(a) as being unpatentable over McAlister, in view of Wu, Verdun, and Main.

Claim 1 recites a double-data rate (DDR) bus system for use in a host-daughtercard interface. The interface is pin compatible with a legacy interface that includes a parallel port utilized by the host to write registers on the legacy daughtercard.

The interface includes daughtercard and host termination logic blocks, coupled to the subset of pins previously used as the parallel port, that redefine the subset of pins as a set of transmit pins, receive pins, and various control pins.

The host termination logic utilizes read and write frames to implement the function of the legacy parallel port to read and write daughtercard registers while the daughtercard termination logic implements DMA and packet transfers utilizing the redefined pins as a DDR bus.

McAlister discloses a method that detects the presence of a non-standard component included in a standard form-factor component card inserted into a standard connector interface and multiplexing the standard interface to different peripheral components, such as the board counterparts of the non-standard component. (2:35-41). This is effected by recognizing that during normal computer system operation, certain pins in the Mini PCI specification are not utilized. (3:57-60). A non-standard component indicates its presence by signaling on lines coupled to redefinable interface pins (4:42). A switch connects non-standard interface pins to a non-standard interface when the non-standard component indicates its presence. (5:1-15).

Wu discloses a system for automatically determining the type of memory, either DDR or SDRAM, provided by the invention. (5:47-67).

Verdun discloses an expansion module having a connector for interfacing with the PCI bus of a portable computer, various connectors for different device, and port replicator for providing the correct protocol to interface with a connected device.

Main discloses a low pin count (LPC) I/O device (superlink) for serving as a docking station or port replicator for a portable PC. The PC includes legacy ports for a mouse, printer, audio, etc. The superlink serializes the data transmissions of different protocols, including the legacy ports,

to reduce the pin count of prior art connectors utilized for docking stations and port replicators. (5:10-55).

The establishment of a prima facie case of obviousness requires that all the claim limitations must be taught or suggested by the prior art. MPEP §2143.03.

There is no teaching or suggestion in the cited references, singly or in combination, of the claimed system where the pins of a parallel port are redefined as a DDR bus and special read/write frames are provided to perform the function of reading and writing daughtercard registers that was previously performed by the parallel port.

In McAlister there is no redefinition of the parallel port pins in the interface. Unutilized pins, which previously performed no function, are used for the non-standard interface. Further, there is no teaching in McAlister of using the redefined pins to perform a function previously defined by the legacy interface, that is reading and writing daughtercard registers.

Wu provides no teaching of redefining pins, it teaches a method for determining the type of DRAM included in the system.

Verdun teaches a port replicator that includes a multi-pin connector on a portable computer and a board having various physical interfaces thereon (Fig. 2). There is no redefinition of pins, as claimed, and no provision for using the redefined pins to perform a function of the legacy parallel port, i.e., reading and writing the daughtercard registers.

Main teaches a port replicator that uses a serial connection between the PC and the port replicator to reduce the pin count required.

Accordingly, there is no teaching or suggestion of the elements and limitations recited in claim 1 and a prima facie case of obviousness has not been established.

Claims 7 recites similar limitations to claim 1 and is thus allowable for the same reasons. The remainder of the claims depend on claims 1 or 7 and are thus allowable, and contain further limitations that make them additionally allowable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (925) 944-3320.

Respectfully submitted,

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